

## DATA SHEET

80C31 $\mu$ /80C51 $\mu$ 

# HIGH SPEED (0 to 42 MHz) SINGLE-CHIP 8 BIT MICROCONTROLLER

- 80C31 $\mu$  : ROMLESS VERSION OF THE 80C51 $\mu$
- 80C31 $\mu$ /80C51 $\mu$ -S : 0 TO 20 MHz
- 80C31 $\mu$ -S/80C51 $\mu$ -25 : 0 TO 25 MHz
- 80C31 $\mu$ /80C51 $\mu$ -30 : 0 TO 30 MHz
- 80C31 $\mu$ /80C51 $\mu$ -36 : 0 TO 36 MHz
- 80C31 $\mu$ /80C51 $\mu$ -40 : 0 TO 40 MHz
- 80C31 $\mu$ /80C51 $\mu$ -42 : 0 TO 42 MHz
- 80C31 $\mu$ /80C51 $\mu$ -L : 0 TO 16 MHz  
WITH 2.7 V < V<sub>CC</sub> < 6 V

## FEATURES

- POWER CONTROL MODES
- 128 x 8 BIT RAM
- 4 K BYTES OF ROM (80C51 $\mu$ )
- 32 PROGRAMMABLE I/O LINES
- TWO 16 BIT TIMER/COUNTER
- 64 K PROGRAM MEMORY SPACE
- FULLY STATIC DESIGN
- BOOLEAN PROCESSOR
- 5 INTERRUPT SOURCES
- PROGRAMMABLE SERIAL PORT
- 64 K DATA MEMORY SPACE
- TEMPERATURE RANGE : COMMERCIAL,  
INDUSTRIAL, AUTOMOTIVE AND MILITARY

## INTRODUCTION

MHS's 80C31 $\mu$  and 80C51 $\mu$  are high performance SCMOS versions of the 8031/8051 NMOS single chip 8 bit  $\mu$ C.

The fully static design of the MHS 80C31 $\mu$ /80C51 $\mu$  allows to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.

The 80C51 $\mu$  retains all the features of the 8051 : 4 K bytes of ROM ; 128 bytes of RAM ; 32 I/O lines ; two 16 bit timers ; a 5-source, 2-level interrupt structure ; a full duplex serial port ; and on-chip oscillator and clock circuits.

In addition, the 80C51 $\mu$  has two software-selectable modes of reduced activity for further reduction in power consumption. In the Idle Mode the CPU is frozen while the RAM, the timers, the serial port, and the interrupt system continue to function. In the Power Down Mode the RAM is saved and all other functions are inoperative.

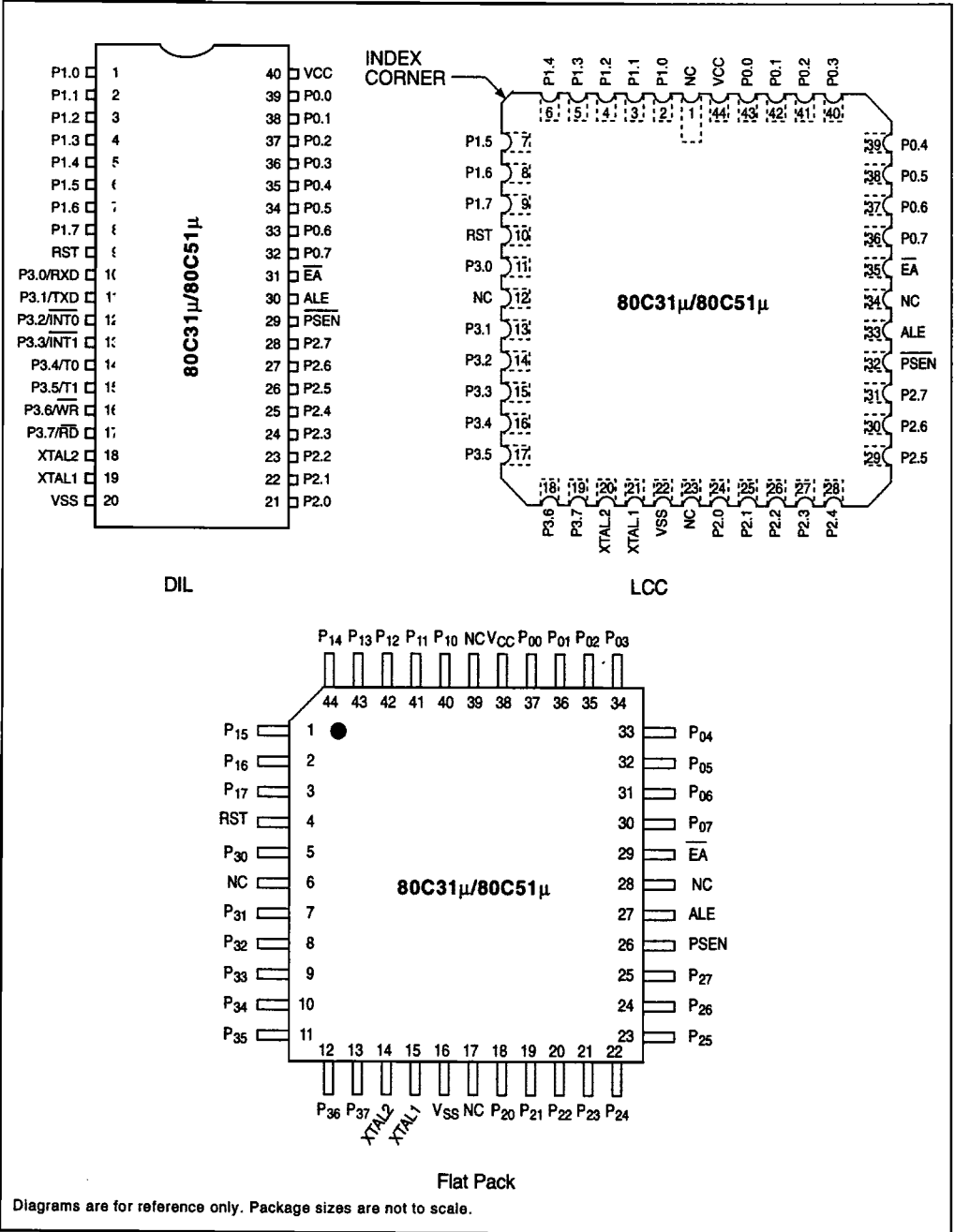
The 80C31 $\mu$  is identical to the 80C51 $\mu$  except that it has no on-chip ROM.

MHS's 80C31 $\mu$ /80C51 $\mu$  are manufactured using SCMOS process which allows them to run from 0 up to 42 MHz with V<sub>CC</sub> = 5 V. MHS's 80C31 $\mu$  and 80C51 $\mu$  are also available at 16 MHz with 2.7 V < V<sub>CC</sub> < 6 V.

5

# INTERFACE

## PIN CONFIGURATION



Diagrams are for reference only. Package sizes are not to scale.

Figure 1.

## PIN DESCRIPTION

### V<sub>SS</sub>

Circuit ground potential

### V<sub>CC</sub>

Supply voltage during normal, Idle, and Power Down operation.

### Port 0

Port 0 is an 8 bit open drain bi-directional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's. Port 0 also outputs the code bytes during program verification in the 80C51 $\mu$ . External pullups are required during program verification. Port 0 can sink eight LS TTL inputs.

### Port 1

Port 1 is an 8 bit bi-directional I/O port with internal pullups. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I<sub>IL</sub>, on the data sheet) because of the internal pullups.

Port 1 also receives the low-order address byte during program verification. In the 80C51 $\mu$ , Port 1 can sink/source three LS TTL inputs. It can drive CMOS inputs without external pullups.

### Port 2

Port 2 is an 8 bit bi-directional I/O port with internal pullups. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I<sub>IL</sub>, on the data sheet) because of the internal pullups. Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8 bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

It also receives the high-order address bits and control signals during program verification in the 80C51 $\mu$ . Port 2 can sink/source three LS TTL inputs. It can drive CMOS inputs without external pullups.

### Port 3

Port 3 is an 8 bit bi-directional I/O port with internal pullups. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I<sub>IL</sub>, on the data sheet) because of the pullups. It also serves the

function of various special features of the MHS 51 Family, as listed below.

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	INT0 (external interrupt 0)
P3.3	INT1 (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	WR (external Data Memory write strobe)
P3.7	RD (external Data Memory read strobe)

Port 3 can sink/source three LS TTL inputs. It can drive CMOS inputs without external pullups.

### RST

A high level on this for two machine cycles while the oscillator is running resets the device. An internal pull-down resistor permits Power-On reset using only a capacitor connected to V<sub>CC</sub>.

### ALE

Address Latch Enable output for latching the low byte of the address during accesses to external memory. ALE is activated as though for this purpose at a constant rate of 1/6 the oscillator frequency except during an external data memory access at which time on ALE pulse is skipped. ALE can sink/source 8 LS TTL inputs. It can drive CMOS inputs without an external pullup.

### PSEN

Program Store Enable output is the read strobe to external Program Memory. PSEN is activated twice each machine cycle during fetches from external Program Memory. (However, when executing out of external Program Memory, two activations of PSEN are skipped during each access to external Data Memory). PSEN is not activated during fetches from internal Program Memory. PSEN can sink/source 8 LS TTL inputs. It can drive CMOS inputs without an external pullup.

### $\overline{EA}$

When EA is held high, the CPU executed out of internal Program Memory (unless the Program Counter exceeds 0FFFFH). When EA is held low, the CPU executes only out of external Program Memory. EA must not be floated.

### XTAL1

Input to the inverting amplifier that forms the oscillator. Receives the external oscillator signal when an external oscillator is used.

### XTAL2

Output of the inverting amplifier that forms the oscillator, and input to the internal clock generator. This pin should be floated when an external oscillator is used.

## FUNCTIONAL DESCRIPTION

## BLOCK DIAGRAM

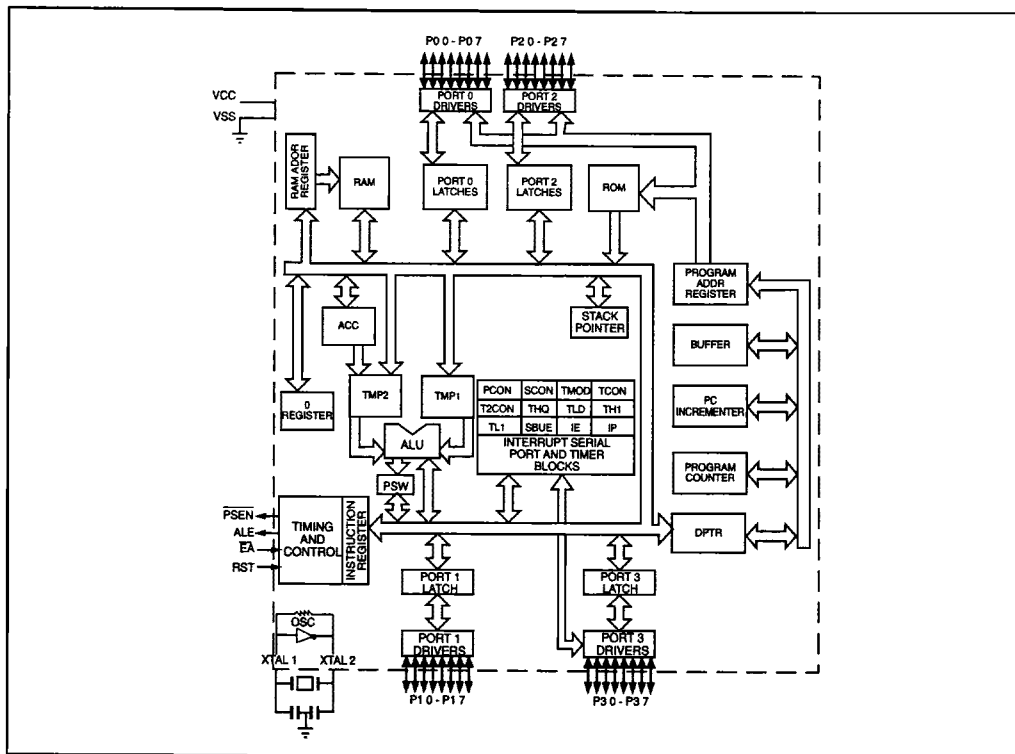


Figure 2.

5

## IDLE AND POWER DOWN OPERATION

Figure 3 shows the internal Idle and Power Down clock configuration. As illustrated, Power Down operation stops the oscillator. Idle mode operation allows the interrupt, serial port, and timer blocks to continue to function while the clock to the CPU is gated off.

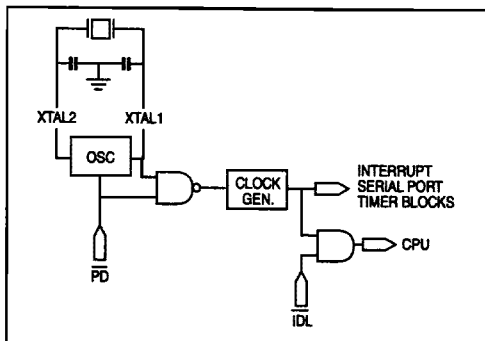


Figure 3 : Idle and Power Down Hardware.

PCON : Power Control Register

(MSB)							(LSB)
SMOD	-	-	-	GF1	GF0	PD	IDL

## Symbol Position Name and Function

SMOD	PCON.7	Double Baud rate bit. When set to a 1, the baud rate is doubled when the serial port is being used in either modes 1, 2 or 3.
-	PCON.6	(Reserved)
-	PCON.5	(Reserved)
-	PCON.4	(Reserved)
GF1	PCON.3	General-purpose flag bit.
GF0	PCON.2	General-purpose flag bit.
PD	PCON.1	Power Down bit. Setting this bit activates power down operation.
IDL	PCON.0	Idle mode bit. Setting this bit activates idle mode operation.

These special modes are activated by software via the Special Function Register, its hardware address is 87H. PCON is not bit addressable.

If 1's are written to PD and IDL at the same time. PD takes precedence. The reset value of PCON is (0XXX0000).

**IDLE MODE**

The instruction that sets PCON.0 is the last instruction executed before the Idle mode is activated. Once in the Idle mode the CPU status is preserved in its entirety : the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM, and all other register maintain their data during Idle. Table 1 describes the status of the external pins during Idle mode.

There are two ways to terminate the Idle mode. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating Idle mode. The interrupt is serviced, and following RETI, the next instruction to be executed will be the one following the instruction that wrote 1 to PCON.0.

The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an enabled interrupt, the service routine can examine the status of the flag bits.

The second way of terminating the Idle is with a hardware reset. Since the oscillator is still running, the hardware reset needs to be active for only 2 machine cycles (24 oscillator periods) to complete the reset operation.

**POWER DOWN MODE**

The instruction that sets PCON.1 is the last executed prior to entering power down. Once in power down, the oscillator is stopped. The contents of the onchip RAM and the Special Function Register is saved during power down mode. A hardware reset is the only way of exiting the power down mode. The hardware reset initiates the Special Function Register (see Table 1).

In the Power Down mode, Vcc may be lowered to minimize circuit power consumption. Care must be taken to ensure the voltage is not reduced until the power down mode is entered, and that the voltage is restored before the hardware reset is applied which frees the oscillator. Reset should not be released until the oscillator has restarted and stabilized.

Table 1 describes the status of the external pins while in the power down mode. It should be noted that if the power down mode is activated while in external program memory, the port data that is held in the Special Function Register P2 is restored to Port 2. If the data is a 1, the port pin is held high during the power down mode by the strong pullup, T1, shown in Figure 4.

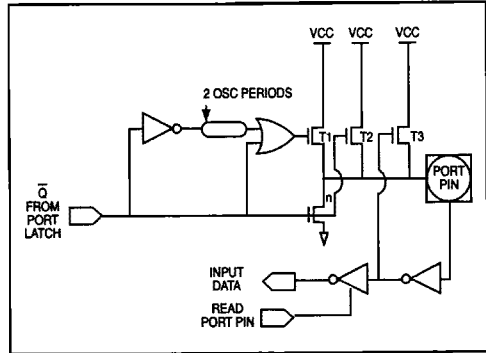


Figure 4 : I/O Buffers in the 80C51μ (Ports 1, 2, 3).

**STOP CLOCK MODE**

Due to static design, the MHS 80C31μ/C51μ clock speed can be reduced until 0 MHz without any data loss in memory or registers. This mode allows step by step utilization, and permits to reduce system power consumption by bringing the clock frequency down to any value. At 0 MHz, the power consumption is the same as in the Power Down Mode.

**I/O PORTS**

The I/O port drive of the 80C51μ is similar to the 8051. The I/O buffers for Ports 1, 2 and 3 are implemented as shown in figure 4.

When the port latch contains a 0, all pFETS in figure 4 are off while the nFET is turned on. When the port latch makes a 0-to-1 transition, the nFET turns off. The strong pullup pFET, T1, turns on for two oscillator periods, pulling the output high very rapidly. As the output line is drawn high, pFET T3 turns on through the inverter to supply the I<sub>OH</sub> source current. This inverter and T3 form a latch which holds the 1 and is supported by T2.

When Port 2 is used as an address port, for access to external program of data memory, any address bit that contains a 1 will have his strong pullup turned on for the entire duration of the external memory access.

5

MODE	PROGRAM MEMORY	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

Table 1 : Status of the external pins during idle and power down modes.

When an I/O pin on Ports 1, 2 or 3 is used as an input, the user should be aware that the external circuit must sink current during the logical 1-to-0 transition. The maximum sink current is specified as ITL under the D.C. Specifications. When the input goes below approximately 2 V, T3 turns off to save ICC current. Note, when returning to a logical 1, T2 is the only internal pullup that is on. This will result in a slow rise time if the user's circuit does not force the input line high.

**OSCILLATOR CHARACTERISTICS**

XTAL1 and XTAL2 are the input and output respectively, of an inverting amplifier which is

configured for use as an on-chip oscillator, as shown in figure 5. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected as shown in figure 6. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the Data Sheet must be observed.

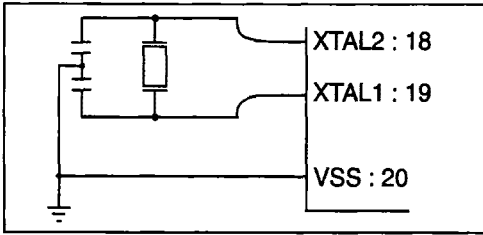


Figure 5 : Crystal Oscillator.

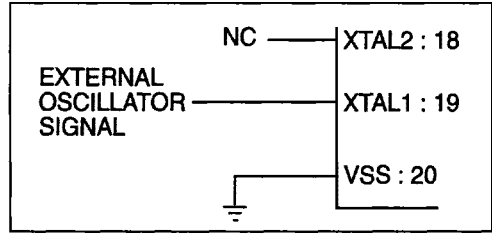


Figure 6 : External Drive Configuration.

5

### 80C51 $\mu$ WITH PROTECTED ROM

MHS provides a new member in the 80C51 $\mu$  Family named "80C51 $\mu$ F" which permits full protection of the internal ROM contents.

With a non protected 80C51 $\mu$ , it is very easy to read out the contents of the internal 4 K bytes of ROM.

Three methods exist, two of them are special test modes and the last one is by means of MOVC instructions.

- **Test mode "VER"** : Using this special test mode, the internal ROM contents are output on port P0 ; the address being applied on ports P2 (AD15...AD8) and P1 (AD7...AD0).
- **Test mode "TMB"** : With this second test mode, the contents of the 80C51 $\mu$  internal bus is presented on port P1 during the PH2 clock phases.
- **Using MOVC instructions** : If EA = 0, and following a reset, the 80C51 $\mu$  fetches its instructions from external program memory. It is then possible to write a small program whose purpose is to dump the internal ROM contents by means of MOVC A, @A + DPTR and MOVC A, @A + PC instructions.

PROM/EPROM (beyond 4 K) and then to dump the internal ROM contents by means of a patch using MOVC instructions.

Thus, if an extra EPROM is necessary, it is advised to ensure that it will contain only constants or tables.

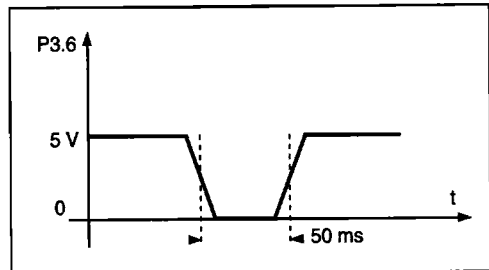
### TEST OF THE ON-CHIP PROGRAM MEMORY

- **Before protection is activated** : The 80C51 $\mu$ F can be tested as any normal 80C51 $\mu$  (using test equipment or any other methods).
- **After protection is activated** : It is then no longer possible to dump the internal ROM contents.

### HOW TO PROGRAM THE PROTECTION MECHANISM

- To burn correctly the fuse a specific configuration of inputs must be settled as below :
  - RST = ALE = 1
  - P3.7 = 1

Furthermore PSEN signal must be tied at + 9 V  $\pm$  5 % level voltage and a pulse must be applied on P3.6 input Port. The timing on P3.6 is shown below :



Time Rise and fall Rise  $\leq$  100  $\mu$ s.

- The electrical schematic shows a typical application to deliver P3.6 signal.

### 80C51 $\mu$ WITH PROGRAM PROTECTION FEATURES

This new version adds ROM protection features in some strategic points of the 80C51 $\mu$ F in order to eliminate the possibility of reading the ROM contents (once the protection has been programmed) by one of the three forementioned methods (VER and TMB test modes, or MOVC instructions).

Nevertheless the customer must note the following :

- Once the protection has been programmed, the 80C51 $\mu$ F program always starts at address 0 in the internal ROM.
- The application program must be self contained in the internal 4 K of ROM, otherwise it would be possible to trap the program counter address in the external

5

## ELECTRICAL CHARACTERISTICS

## ABSOLUTE MAXIMUM RATINGS\*

Ambiant Temperature Under Bias :

C = commercial..... 0°C to + 70°C  
 I = Industrial..... - 40°C to 85°C  
 Storage Temperature..... - 65°C to + 150°C  
 Voltage on VCC to VSS..... - 0.5 V to + 7 V  
 Voltage on Any Pin to VSS..... - 0.5 V to VCC + 0.5 V  
 Power Dissipation..... 1 W

\*\* This value is based on the maximum allowable die temperature and the thermal resistance of the package

## \* Notice :

Stresses above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC PARAMETERS

TA = 0°C to 70°C ; VCC = 0 V ; VCC = 5 V +/- 10 % ; F = 0 to 42 MHz

TA = - 40°C + 85°C ; VCC = 0 V ; VCC = 5 V +/- 10 % ; F = 0 to 36 MHz

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
VIL	Input Low Voltage	- 0.5	0.2 Vcc - 0.1	V	
VIH	Input High Voltage (Except XTAL and RST)	0.2 Vcc + 1.4	Vcc + 0.5	V	
VIH1	Input High Voltage (for XTAL and RST)	0.7 Vcc	Vcc + 0.5	V	
VOL	Output Low Voltage (Port 1, 2 and 3)		0.3	V	IOL = 100 μA
			0.45	V	IOL = 1.6 mA (note 2)
			1.0	V	IOL = 3.5 mA
VOL1	Output Low Voltage (Port 0, ALE, PSEN)		0.3	V	IOL = 200 μA
			0.45	V	IOL = 3.2 mA (note 2)
			1.0	V	IOL = 7.0 mA
VOH	Output High Voltage Port 1, 2 and 3	Vcc - 0.3		V	IOH = - 10 μA
		Vcc - 0.7		V	IOH = - 30 μA
		Vcc - 1.5		V	IOH = - 60 μA VCC = 5 V ± 10 %
VOH1	Output High Voltage (Port 0, ALE, PSEN)	Vcc - 0.3		V	IOH = - 200 μA
		Vcc - 0.7		V	IOH = - 3.2 mA
		Vcc - 1.5		V	IOH = - 7.0 mA VCC = 5 V ± 10 %
IIL	Logical 0 Input Current (Ports 1, 2 and 3)		- 50	μA	Vin = 0.45 V
ILI	Input leakage Current		+/- 10	μA	0.45 < Vin < Vcc
ITL	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)		- 650	μA	Vin = 2.0 V
IPD	Power Down Current		50	μA	Vcc = 2.0 V to 5.5 V (note 1)
RRST	RST Pulldown Resistor	50	200	KOhm	
CIO	Capacitance of I/O Buffer		10	pF	fc = 1 MHz, Ta = 25°C
ICC	Power Supply Current Active Mode	20 MHz	32		Vcc = 5.5 V (note 1)
		25 MHz	40		
		30 MHz	47		
		36 MHz	54		
		40 MHz	59		
		42 MHz	61		
	Idle Mode	20 MHz	11		
		25 MHz	12		
		30 MHz	14		
		36 MHz	15		
		40 MHz	16		
		42 MHz	17		



**ABSOLUTE MAXIMUM RATINGS\***

Ambient Temperature Under Bias :  
 A = Automotive ..... - 40°C to + 125°C  
 Storage Temperature ..... - 65°C to + 150°C  
 Voltage on VCC to VSS ..... - 0.5 V to + 7 V  
 Voltage on Any Pin to VSS ..... - 0.5 V to VCC + 0.5 V  
 Power Dissipation ..... 1 W  
 \*\* This value is based on the maximum allowable die temperature and the thermal resistance of the package

**\* Notice :**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**DC PARAMETERS**

TA = - 40°C + 125°C ; VSS = 0 V ; VCC = 5 V +/- 10 % ; F = 0 to 36 MHz

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
VIL	Input Low Voltage	- 0.5	0.2 Vcc - 0.1	V	
VIH	Input High Voltage (Except XTAL and RST)	0.2 Vcc + 1.4	Vcc + 0.5	V	
VIH1	Input High Voltage (for XTAL and RST)	0.7 Vcc	Vcc + 0.5	V	
VOL	Output Low Voltage (Port 1, 2 and 3)		0.3 0.45 1.0	V	IOL = 100 μA IOL = 1.6 mA (note 2) IOL = 3.5 mA
VOL1	Output Low Voltage (Port 0, ALE, PSEN)		0.3 0.45 1.0	V	IOL = 200 μA IOL = 3.2 mA (note 2) IOL = 7.0 mA
VOH	Output High Voltage Port 1, 2 and 3	Vcc - 0.3		V	IOH = - 10 μA
		Vcc - 0.7		V	IOH = - 30 μA
		Vcc - 1.5		V	IOH = - 60 μA VCC = 5 V ± 10 %
VOH1	Output High Voltage (Port 0, ALE, PSEN)	Vcc - 0.3		V	IOH = - 200 μ
		Vcc - 0.7		V	IOH = - 3.2 mA
		Vcc - 1.5		V	IOH = - 7.0 mA VCC = 5 V ± 10 %
IIL	Logical 0 Input Current (Ports 1, 2 and 3)		- 75	μA	Vin = 0.45 V
ILI	Input leakage Current		+/- 10	μA	0.45 < Vin < Vcc
ITL	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)		- 750	μA	Vin = 2.0 V
IPD	Power Down Current		75	μA	Vcc = 2.0 V to 5.5 V (note 1)
RRST	RST Pulldown Resistor	50	200	KOhm	
CIO	Capacitance of I/O Buffer		10	pF	fc = 1 MHz, Ta = 25°C
ICC	Power Supply Current Active Mode 20 MHz		34		Vcc = 5.5 V (note 1)
		25 MHz	40		
		30 MHz	47		
		36 MHz	54		
	Idle Mode	20 MHz	11		
		25 MHz	12		
		30 MHz	14		
	36 MHz	15			

**5**

**ABSOLUTE MAXIMUM RATINGS\***

Ambiant Temperature Under Bias :

M = Military ..... - 55°C to + 125°C

Storage Temperature..... - 65°C to + 150°C

Voltage on VCC to VSS..... - 0.5 V to + 7 V

Voltage on Any Pin to VSS..... - 0.5 V to VCC + 0.5 V

Power Dissipation..... 1 W

\*\* This value is based on the maximum allowable die temperature and the thermal resistance of the package

**\* Notice :**

Stresses above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**DC PARAMETERS**

TA = - 55°C + 125°C ; Vss = 0 V ; Vcc = 5 V +/- 10 % ; F = 0 to 36 MHz

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
VIL	Input Low Voltage	- 0.5	0.2 Vcc - 0.1	V	
VIH	Input High Voltage (Except XTAL and RST)	0.2 Vcc + 1.4	Vcc + 0.5	V	
VIH1	Input High Voltage (for XTAL and RST)	0.7 Vcc	Vcc + 0.5	V	
VOL	Output Low Voltage (Port 1, 2 and 3)		0.45	V	IOL = 1.6 mA (note 2)
VOL1	Output Low Voltage (Port 0, ALE, PSEN)		0.45	V	IOL = 3.2 mA (note 2)
VOH	Output High Voltage (Port 1, 2 and 3)	0.9 Vcc		V	IOH = - 10 μA
VOH1	Output High Voltage (Port 0, ALE, PSEN)	0.9 Vcc		V	IOH = - 80 μA
IIL	Logical 0 Input Current (Ports 1, 2 and 3)		- 75	μA	Vin = 0.45 V
ILI	Input leakage Current		+/- 10	μA	0.45 < Vin < Vcc
ITL	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)		- 750	μA	Vin = 2.0 V
IPD	Power Down Current		75	μA	Vcc = 2.0 V to 5.5 V (note 1)
RRST	RST Pulldown Resistor	50	200	KOhm	
CIO	Capacitance of I/O Buffer		10	pF	fc = 1 MHz, Ta = 25°C
ICC	Power Supply Current Active Mode 20 MHz 25 MHz 30 MHz 36 MHz Idle Mode 20 MHz 25 MHz 30 MHz 36 MHz		32 40 47 54 11 12 14 15		Vcc = 5.5 V (note 1)

5

**ABSOLUTE MAXIMUM RATINGS\***

Ambient Temperature Under Bias :  
 C = commercial ..... 0°C to + 70°C  
 Storage Temperature ..... - 65°C to + 150°C  
 Voltage on VCC to VSS..... - 0.5 V to + 7 V  
 Voltage on Any Pin to VSS ..... - 0.5 V to VCC + 0.5 V  
 Power Dissipation..... 1 W  
 \*\* This value is based on the maximum allowable die temperature and the thermal resistance of the package

**\* Notice :**

*Stresses above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

**DC CHARACTERISTICS**

T<sub>A</sub> = 0° to 70°C ; V<sub>CC</sub> = 2.7 V to 6 V ; V<sub>SS</sub> = 0 V ; F = 0 to 16 MHz

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
VIL	Input Low Voltage	- 0.5	0.2 V <sub>CC</sub> - 0.1	V	
VIH	Input High Voltage (Except XTAL and RST)	0.2 V <sub>CC</sub> + 1.4	V <sub>CC</sub> + 0.5	V	
VIH1	Input High Voltage to XTAL1	0.7 V <sub>CC</sub>	V <sub>CC</sub> + 0.5	V	
VIH2	Input High Voltage to RST for Reset	0.7 V <sub>CC</sub>	V <sub>CC</sub> + 0.5	V	
VPD	Power Down Voltage to V <sub>CC</sub> in PD Mode	2.0	6.0	V	
VOL	Output Low Voltage (Ports 1, 2, 3)		0.45	V	IOL = 0.8 mA (note 2)
VOL1	Output Low Voltage Port 0, ALE, PSEN		0.45	V	IOL = 1.6 mA (note 2)
VOH	Output High Voltage Ports 1, 2, 3	0.9 V <sub>CC</sub>		V	IOH = - 10 μA
VOH1	Output High Voltage (Port 0 in External Bus Mode), ALE, PSEN	0.9 V <sub>CC</sub>		V	IOH = - 80 μA
IIL	Logical 0 Input Current Ports 1, 2, 3		- 50	μA	Vin = 0.45 V
ILI	Input Leakage Current		± 10	μA	0.45 < Vin < V <sub>CC</sub>
ITL	Logical 1 to 0 Transition Current (Ports 1, 2, 3)		- 650	μA	Vin = 2.0 V
IPD	Power Down Current		50	μA	V <sub>CC</sub> = 2 V to 6 V (note 1)
RRST	RST Pulldown Resistor	50	200	kΩ	
CIO	Capacitance of I/O Buffer		10	pF	fc = 1 MHz, T <sub>A</sub> = 25°C

**5**

**MAXIMUM I<sub>CC</sub> (mA)**

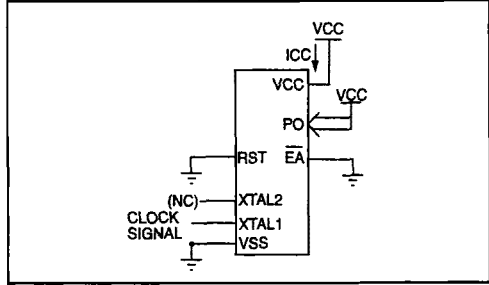
FREQUENCY/V <sub>CC</sub>	OPERATING (NOTE 1)					IDLE (NOTE 1)				
	2.7 V	3 V	3.3 V	5 V	5.5 V	2.7 V	3 V	3.3 V	5 V	5.5 V
1 MHz	0.8 mA	1 mA	1.1 mA	1.5 mA	1.8 mA	400 μA	500 μA	600 μA	800 μA	1 mA
6 MHz	4 mA	5 mA	6 mA	8.2 mA	10 mA	1.5 mA	1.7 mA	2 mA	3 mA	4 mA
12 MHz	8 mA	10 mA	12 mA	17 mA	19 mA	2.5 mA	3 mA	3.5 mA	5.5 mA	7 mA
16 MHz	10 mA	12 mA	14 mA	21 mA	24 mA	3 mA	3.8 mA	4.5 mA	7 mA	9 mA

**Note 1 :** ICC is measured with all output pins disconnected ; XTAL1 driven with TCLCH, TCHCL = 5 ns, VIL = VSS + .5 V, VIH = VCC - .5 V ; XTAL2 N.C. ; EA = RST = Port 0 = VCC. ICC would be slightly higher if a crystal oscillator used.

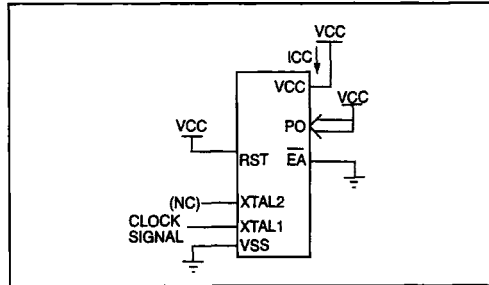
Idle ICC is measured with all output pins disconnected ; XTAL1 driven with TCLCH, TCHCL = 5 ns, VIL = VSS + 5 V, VIH = VCC - .5 V ; XTAL2 N.C ; Port 0 = VCC ; EA = RST = VSS.

Power Down ICC is measured with ε ' output pins disconnected ; EA = PORT 0 = VCC ; XTAL2 N.C. ; RST = VSS.

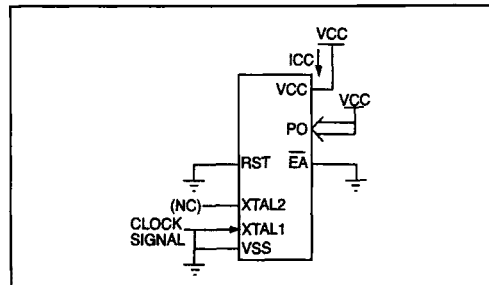
**Note 2 :** Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the VOLs of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operations. In the worst cases (capacitive loading 100 pF), the noise pulse on the ALE line may exceed 0.45 V with maxi VOL peak 0.6 V. A Schmitt Trigger use is not necessary.



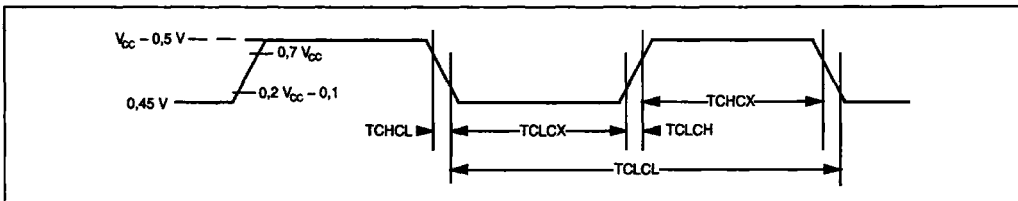
**Figure 7 : ICC Test Condition, Idle Mode.**  
All other pins are disconnected.



**Figure 8 : ICC Test Condition, Active Mode.**  
All other pins are disconnected.



**Figure 9 : ICC Test Condition, Power Down Mode.**  
All other pins are disconnected.



**Figure 10 : Clock Signal Waveform for ICC Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns.**

**EXPLANATION OF THE AC SYMBOL**

Each timing symbol has 5 characters. The first character is always a "T" (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

**Example :**

TAVLL = Time for Address Valid to ALE low.  
 TLLPL = Time for ALE low to PSEN low.

- |  |                                    |
|--|------------------------------------|
| A : Address.                               | Q : Output data.                   |
| C : Clock.                                 | R : READ signal.                   |
| D : Input data.                            | T : Time.                          |
| H : Logic level HIGH.                      | V : Valid.                         |
| I : Instruction (program memory contents). | W : WRITE signal.                  |
| L : Logic level LOW, or ALE.               | X : No longer a valid logic level. |
| P : PSEN.                                  | Z : Float.                         |

**AC PARAMETERS :**

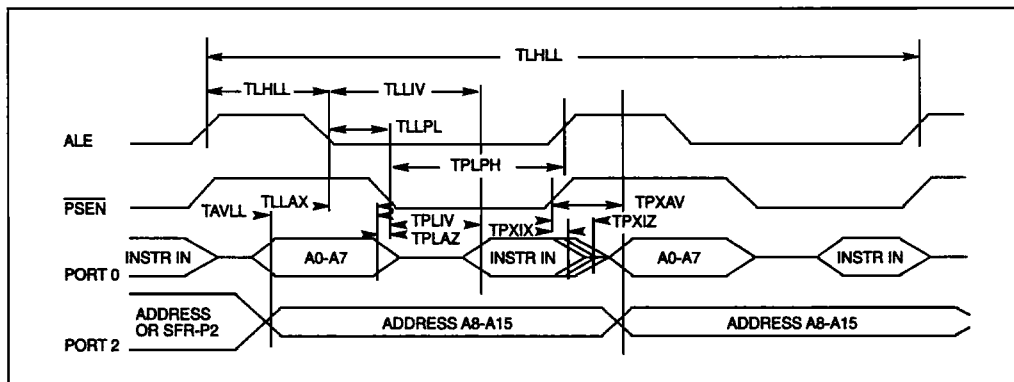
TA = 0 to + 70°C ; VSS = 0 V ; VCC = 5 V +/- 10 % ; F = 0 to 42 MHz  
 TA = - 40° + 85°C ; VSS = 0 V ; 2.7 V < VCC < 6 V ; F = 0 to 16 MHz  
 TA = - 55° + 125°C ; VSS = 0 V ; VCC = 5 V +/- 10 % ; F = 0 to 36 MHz  
 (Load Capacitance for PORT 0, ALE and PSEN = 100 pF ; Load Capacitance for all other outputs = 80 pf)

**EXTERNAL PROGRAM MEMORY CHARACTERISTICS**

SYMBOL	PARAMETER	16 MHz		20 MHz		25 MHz		30 MHz		36 MHz		40 MHz		42 MHz	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
TLHLL	ALE Pulse Width	110		90		70		60		50		40		35	
TAVLL	Address valid to ALE	40		30		20		15		10		9		8	
TLLAX	Address Hold After ALE	35		35		35		35		35		30		25	
TLLIV	ALE to valid instr in		185		170		130		100		80		70		65
TLLPL	ALE to PSEN	45		40		30		25		20		15		13	
TPLPH	PSEN pulse Width	165		130		100		80		75		65		60	
TPLIV	PSEN to valid instr in		125		110		85		65		50		45		40
TPXIX	Input instr Hold After PSEN	0		0		0		0		0		0		0	
TPXIZ	Input instr Float After PSEN		50		45		35		30		25		20		15
TPXAV	PSEN to Address Valid	55		42		32		25		20		17		15	
TAVIV	Address to Valid instr in		230		210		170		130		90		80		75
TPLAZ	PSEN low to Address Float		10		10		8		6		5		5		5

5

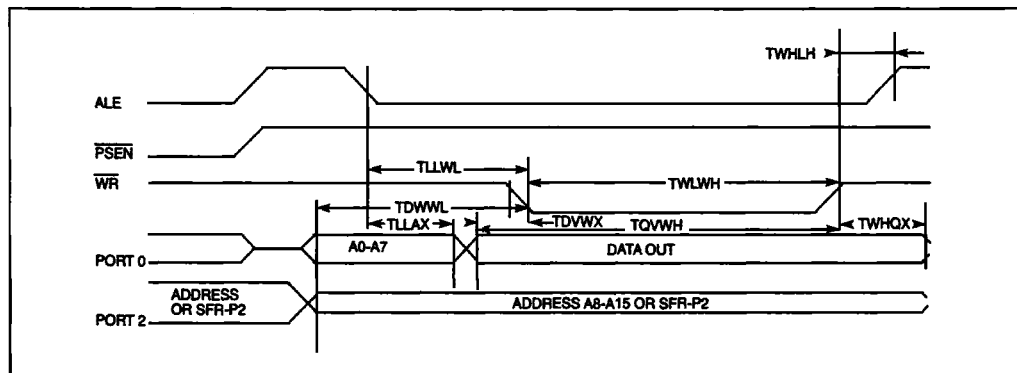
**EXTERNAL PROGRAM MEMORY READ CYCLE**



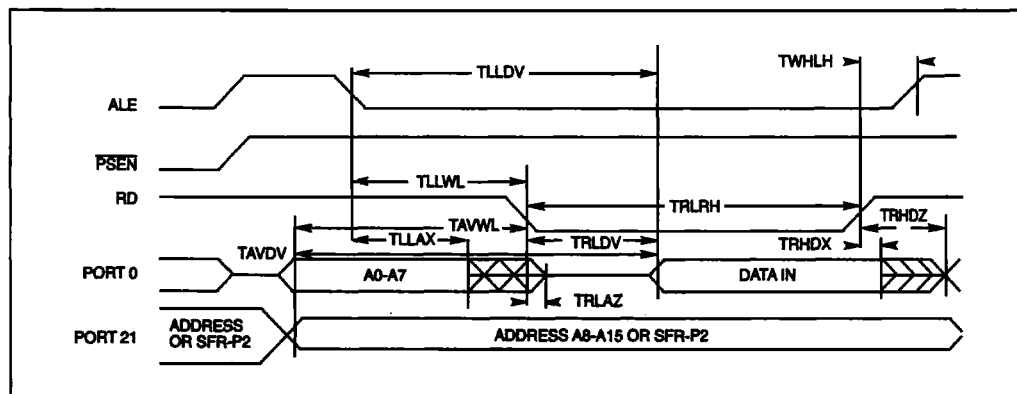
EXTERNAL DATA MEMORY CHARACTERISTICS

SYMBOL	PARAMETER	16 MHz		20 MHz		25 MHz		30 MHz		36 MHz		40 MHz		42 MHz	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
TRLRH	RD pulse Width	340		270		210		180		120		100		90	
TWLWH	WR pulse Width	340		270		210		180		120		100		90	
TLLAX	Address Hold After ALE	85		85		70		55		35		30		25	
TRLDV	RD to Valid In		240		210		175		135		110		90		80
TRHDX	Data hold after RD	0		0		0		0		0		0		0	
TRHDZ	Data float after RD		90		90		80		70		50		45		40
TLLDV	ALE to Valid Data In		435		370		350		235		170		150		140
TAVDV	Address to Valid Data IN		480		400		300		260		190		180		175
TLLWL	ALE to WR or RD	150	250	135	170	120	130	90	115	70	100	60	95	55	90
TAVWL	Address to WR or RD	180		180		140		115		75		65		60	
TQVWX	Data valid to WR transition	35		35		30		20		15		10		8	
TQVWH	Data Setup to WR transition	380		325		250		215		170		160		150	
TWHQX	Data Hold after WR	40		35		30		20		15		10		8	
TRLAZ	RD low to Address Float		0		0		0		0		0		0		0
TWHLH	RD or WR high to ALE high	35	90	35	60	25	45	20	40	20	40	15	35	13	33

EXTERNAL DATA MEMORY WRITE CYCLE



EXTERNAL DATA MEMORY READ CYCLE

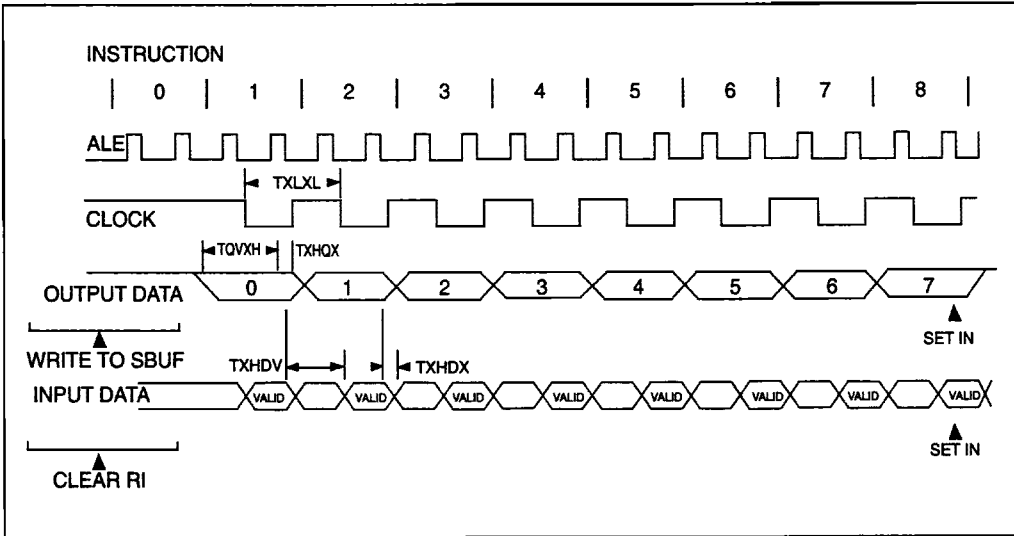


5

SERIAL PORT TIMING – SHIFT REGISTER MODE

SYMBOL	PARAMETER	16 MHz		20 MHz		25 MHz		30 MHz		36 MHz		40 MHz		42 MHz	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
TXLXL	Serial Port Clock Cycle Time	750		600		480		400		330		250		230	
TQVXH	Output Data Setup to Clock Rising Edge	563		480		380		300		220		170		150	
TXHQX	Output Data Hold after Clock Rising Edge	63		90		65		50		45		35		30	
TXHDX	Input Data Hold after Clock Rising Edge	0		0		0		0		0		0		0	
TXHDV	Clock Rising Edge to Input Data Valid		563		450		350		300		250		200		180

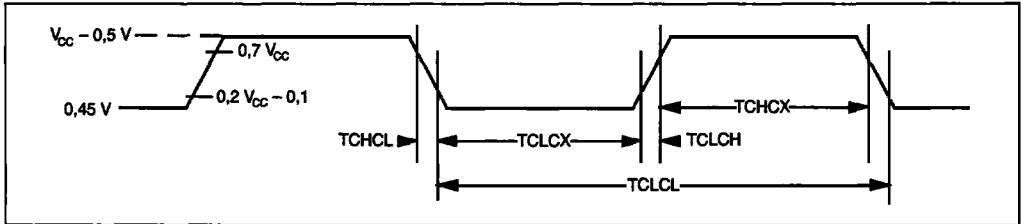
SHIFT REGISTER TIMING WAVEFORMS



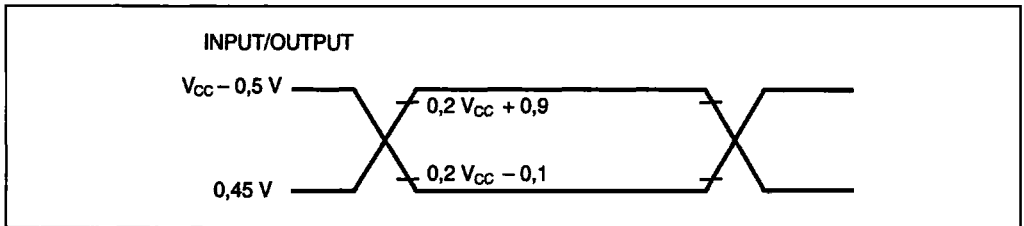
**EXTERNAL CLOCK DRIVE CHARACTERISTICS (XTAL1)**

SYMBOL	PARAMETER	MIN	MAX	UNIT
FCLCL	Oscillator Frequency		42	Mhz
TCLCL	Oscillator period	23.8		ns
TCHCX	High Time	5		ns
TCLCX	Low Time	5		ns
TCLCH	Rise Time		5	ns
TCHCL	Fall Time		5	ns

**EXTERNAL CLOCK DRIVE WAVEFORMS**



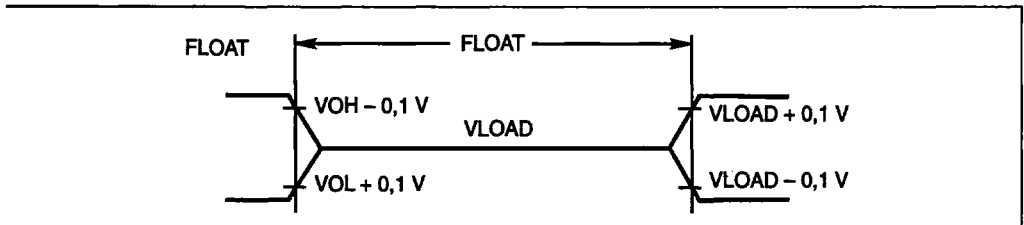
**AC TESTING INPUT/OUTPUT WAVEFORMS**



AC inputs during testing are driven at  $V_{CC} - 0.5$  for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at  $V_{IH}$  min for a logic "1" and  $V_{IL}$  max for a logic "0".

**5**

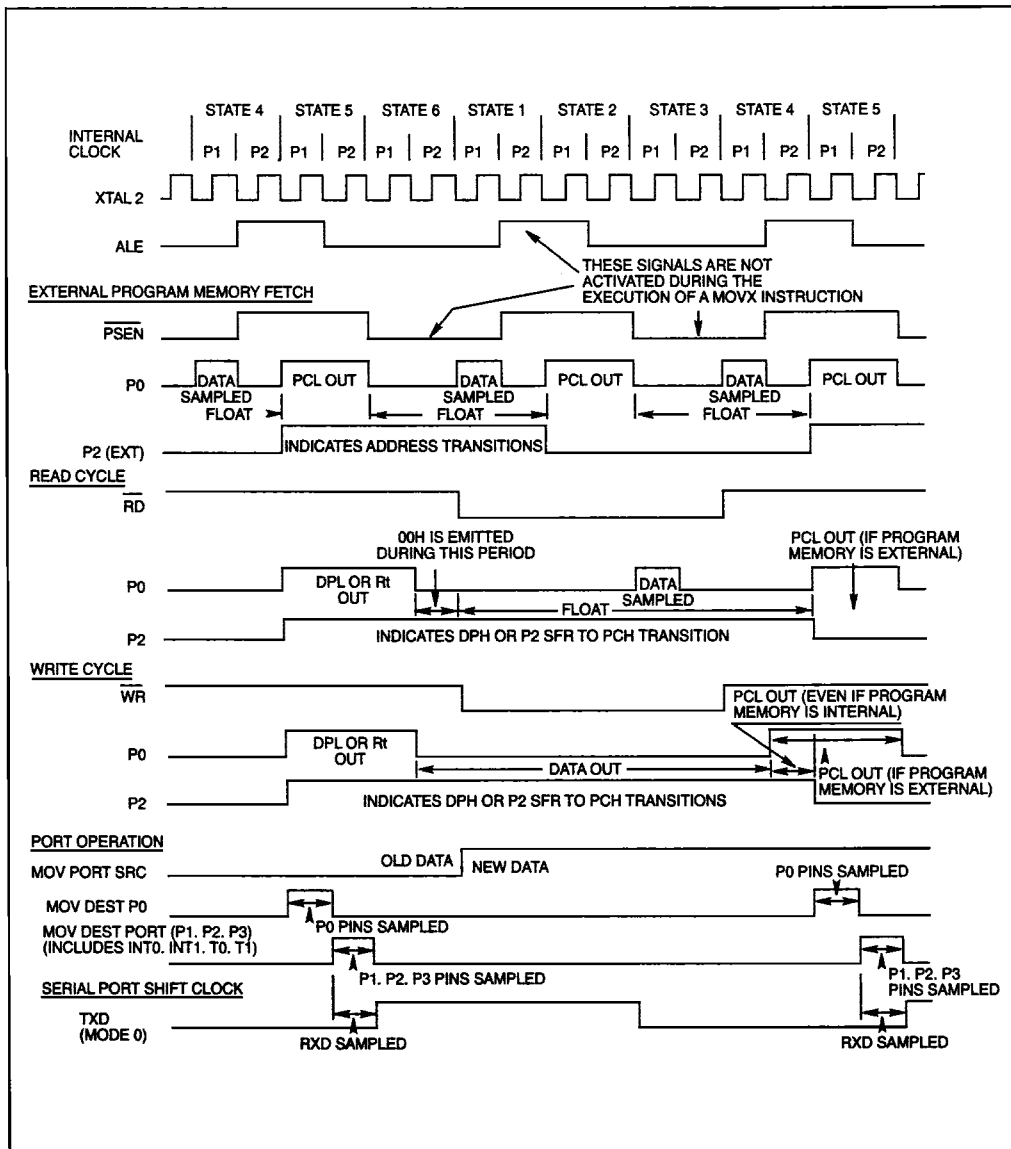
**FLOAT WAVEFORMS**



For timing purposes as port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded  $VOH/VOL$  level occurs.  $I_{OL}/I_{OH} \geq \pm 20$  mA.



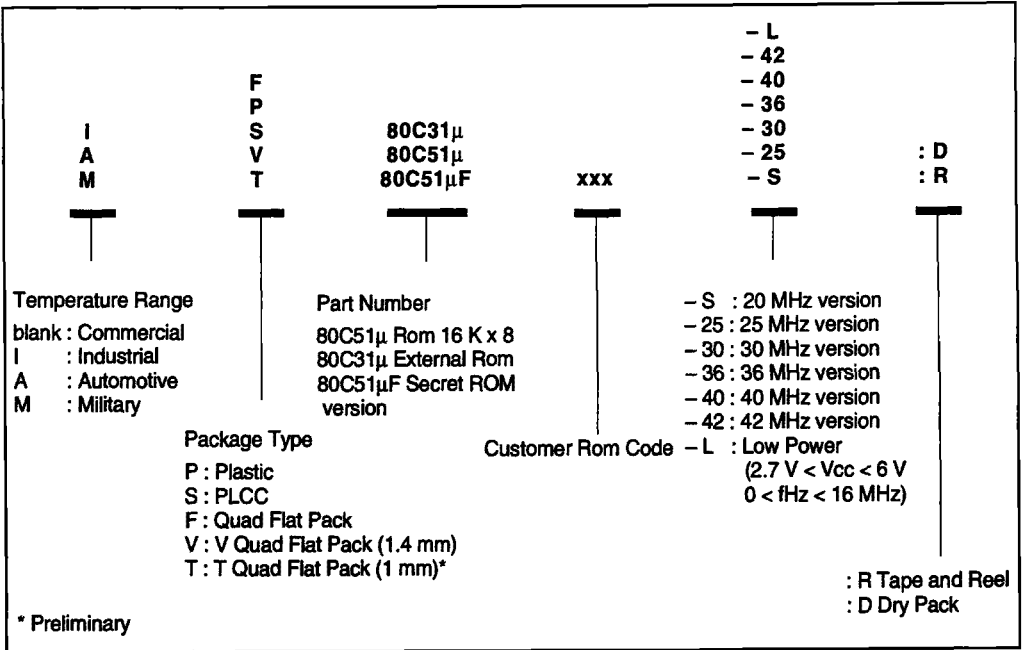
CLOCK WAVEFORMS



5

This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though ( $T_A = 25^\circ\text{C}$  fully loaded) RD and WR propagation delays are approximately 50 ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

## ORDERING INFORMATION



5